29. (New) The apparatus of claim 28, wherein:

z is not equal to m.

30. (New) The apparatus of claim 24, wherein the selected physical rename register is selected from the plurality of n registers, which includes multiple registers of both the first type and the second type.

REMARKS and ARGUMENTS

Claims 9-22 stand allowed. However, it has come to the attention of the Applicants that a copy of the International Search Report for the corresponding PCT case was not submitted to this Examiner. Thus, Applicants are concurrently submitting herewith an IDS with the references cited in the International Search Report (ISR) along with this Response.

The ISR cites three references designated as "X" references: US 6,047,369 (Colwell); US 5,689,720 (Nguyen); and US 6,393,552 (Eikemeyer). During prosecution of this case, the Eikemeyer reference was cited by the Examiner in this case, and the claims were ultimately allowed over the Eikemeyer reference. However, it does not appear that the Colwell and Nguyen references were considered during prosecution of the US case.

Colwell discloses renaming flags within a register alias table to increase processor parallelism by providing a larger physical register set than would otherwise be provided (abstract, col. 3 line 65 – col. 4 line 10). The register alias table (RAT) is for renaming

integer flag bits and also for renaming floating point flag bits. The RAT also renames integer registers (col. 6 lines 63-66). A first column of each entry in the integer RAT indicates the size of the data represented by the entry. The size column may indicate either storage of a 32-bit width of data, a 16-bit width of data or an 8-bit width for each of the 12 entries of a RAM array (col. 13 lines 41-48). The integer RAT is logically separated into an upper portion and a lower portion for the integer registers that use partial width sizes, to eliminate RAT stalls upon renaming registers of partial widths (col. 14 lines 51-66).

Nguyen appears to disclose a microprocessor architecture capable of concurrent execution of instructions obtained from an instruction store. An instruction FIFO is provided for buffering instruction sets in a plurality of instruction set buffers including a first buffer and a second buffer (col. 4 lines 10-18). The disclosure incorporates multiple register files within the register file unit that are generalized, typed and capable of multiple register file functions (col. 5 lines 2-5). A register rename unit selects source registers for access in the execution of instructions and substitutes temporary buffer register references for register file register references in he case of out-of-order executed instructions. The substitution of a temporary buffer destination register reference is determined by the location of the corresponding instruction within the pending register sets (col. 49 lines 27-53).

However, neither Colwell nor Nguyen discloses, suggests, nor teaches two groups of physical registers of different respective lengths and a rename map table for mapping accesses from a predicate register to one or other of the respective groups of registers dependent on a bit-length of the access.

Amendments are presented herein to distinguish the claims over the Colwell and Nguyen references.

Accordingly, Applicants respectfully submit that the applicable rejections have been overcome and must all be withdrawn. Applicants reserve all rights with respect to the application of the doctrine equivalents. Applicant respectfully requests that a timely Notice of Allowance be issued in this case. If the Examiner feels that an interview would help to resolve any remaining issues in the case, the Examiner is invited to contact Shireen Bacon of Intel, at (512) 732-3917.

Please charge any shortages and credit any overcharges to our Deposit Account No. 02-2666.

Respectfully submitted,

Dated: December 19, 2006

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